



2006-01-01

Effect of Step Sintering on Breakdown Voltage of Varistors Prepared from Nanomaterials

Suresh Pillai

Dublin Institute of Technology, suresh.pillai@dit.ie

Declan McCormack

John Kelly

Ramesh Raghavendra

Follow this and additional works at: <http://arrow.dit.ie/cenresart>

 Part of the [Materials Science and Engineering Commons](#)

Recommended Citation

Pillai, S.,* Kelly, J., McCormack, D. E., and Raghavendra, R. Effect of step sintering on the breakdown voltage of varistors, *Advances in applied ceramics*.. 105, 2006, 158-160.

This Article is brought to you for free and open access by the Crest: Centre for Research in Engineering Surface Technology at ARROW@DIT. It has been accepted for inclusion in Articles by an authorized administrator of ARROW@DIT. For more information, please contact yvonne.desmond@dit.ie, arrow.admin@dit.ie.



This work is licensed under a [Creative Commons Attribution-NonCommercial-Share Alike 3.0 License](#)



Effect of step sintering on breakdown voltage of varistors prepared from nanomaterials by sol gel route

S. C. Pillai*^{1,2}, J. M. Kelly², D. E. McCormack³ and R. Ramesh⁴

ZnO varistor materials were prepared by a sol gel route with subsequent drying and calcination. Varistor discs fabricated from these materials were subjected to a two step sintering schedule. Therefore in a typical experiment, the samples were heated to 1000°C, then allowed to cool for over 30 min to 900°C and held there for 6 h. The results were compared with commercial varistor samples sintered in a similar way. Considerably higher breakdown voltages were obtained for the varistors made from nanosample ($1192 \pm 30 \text{ V mm}^{-1}$) compared with the commercial samples ($723 \pm 30 \text{ V mm}^{-1}$) sintered under the same experimental conditions. The sintered materials were characterised by X-ray diffraction (XRD), field emission scanning electron microscopy (FESEM) and density measurements.

Keywords: ZnO, Varistors, Sintering, Nano, Grain growth, Dopants

Introduction

ZnO varistors are used as surge suppressors in most of the areas of electronic and communication technologies.^{1–5} These are conventionally prepared from ZnO and other additives (Bi_2O_3 , Sb_2O_3 , CoO , MnO , Cr_2O_3 , NiO and Al_2O_3) using a solid state reaction by plastification, pelletisation and sintering.^{1,2} The pressed discs are then sintered at 1100–1250°C. They are characterised by a threshold voltage (breakdown voltage or V_c), where the transition from linear to non-linear mode occurs.^{1,2} It is well known that the breakdown voltage of a sintered ceramic body is proportional to the number of grain and grain boundaries formed in between the electrodes.^{5,7} A high performing device in a smaller dimension might therefore be prepared by employing nanosize precursor materials.^{5–8} Additionally, nanoparticles can be sintered at a lower temperature compared with the coarse grained ceramics.

A novel sintering procedure has been reported recently for the sintering of nanocrystalline Y_2O_3 .⁹ This method uses two steps in the heating schedule. The pellet is first heated to a higher temperature to achieve an intermediate density, then cooled down and held at a slightly lower temperature for several hours. In the present report, a similar approach is used for sintering the varistor nanopowder prepared by a sol gel route and it is compared with commercial samples

processed in a similar way. It should also be noted that this type of thermal processing has earlier been studied on ZnO varistor powder prepared by a modified Pechini polymeric complex method.^{10,11}

Experimental

Nanovaristor powders have been prepared by a sol gel reaction using zinc acetate dihydrate, oxalic acid, cobalt acetate, nickel acetate, aluminium nitrate, chromium nitrate and magnesium acetate. A detailed experimental procedure for making varistors from nanopowders has been explained in previous articles by the authors.^{5,6} Varistor discs produced were sintered using a step sintering procedure.^{9–11} The samples were heated to 1000°C and held at this temperature for 0 h after which the temperature was lowered (cooling time 30 min) to 900°C for 6 h and then left to cool down room temperature. Conventional sintering has been performed for 1000°C (held at this temperature for 2 h).

Current–voltage characteristics (from 0.1 μA to 10 mA) were measured using a Keithley instrument (model 2410). The breakdown voltage V_c is taken as the voltage at a current density of 1 mA. Scanning electron microscopy (SEM) characterisations were carried out using a Hitachi S-4300 field emission scanning electron microscopy (FESEM) instrument, which was operated at 5.0 or 20.0 kV. Samples for analysis were mounted on aluminium stubs and coated with graphite.

Results

Powder characterisations

The powder obtained after the calcination at 500°C was analysed using X-ray powder diffraction and TEM. Broadening of the X-ray band allowed an estimate of the average particle size as $15 \pm 3 \text{ nm}$ using the Scherrer

¹Centre for Research in Engineering and Surface Technology (CREST), FOGAS Institute, Dublin Institute of Technology, Camden Row, Dublin 8, Ireland

²Department of Chemistry, University of Dublin Trinity College, Dublin 2, Ireland

³School of Chemical and Pharmaceutical Sciences, Dublin Institute of Technology, Kevin Street, Dublin 8, Ireland

⁴Littelfuse Ireland Ltd., Ecco Road, Dundalk, Ireland

*Corresponding author, email suresh.pillai@dit.ie

equation. Transmission electron microscopy studies also showed a similar average particle size of 19 ± 3 nm.

Densification

The nanopowder was pelletised, attaining a presintered density of $49 \pm 2\%$ theoretical value (commercial sample; $65 \pm 2\%$ theoretical density). Table 1 shows the densification values of the sintered discs by two sintering schedules. Almost the same densification was obtained for nanovaristors sintered by conventional or step sintering procedure. Note that the densification of the commercial (micrometre sized) material is poor under above sets of sintering conditions used here demonstrating the advantage of working with nanomaterials. Commercial samples are conventionally sintered at $1100\text{--}1250^\circ\text{C}$. Field emission scanning electron microscopy studies show that average grain sizes of 1.60 ± 0.05 and 2.00 ± 0.05 μm have been obtained by step sintering and conventional sintering techniques respectively.

Phase analysis

During sintering, different dopants migrate either towards the grain boundary or towards the grains. Various phases are formed in such a way that the grain is conducting and the grain boundary is insulating. It is known that the $\text{ZnO-Bi}_2\text{O}_3\text{-Sb}_2\text{O}_3$ system processed conventionally forms a pyrochlore phase $\text{Zn}_2\text{Bi}_3\text{Sb}_3\text{O}_{14}$ at lower temperatures ($<650^\circ\text{C}$) and that this further reacts with ZnO forming a spinel ($\text{Zn}_7\text{Sb}_2\text{O}_{12}$) above 900°C .^{1,2,5} Usually, there are three major phases identified in a typical ZnO microstructure:^{1,2,5} ZnO grains, Bi rich areas (Bi_2O_3) and spinel ($\text{Zn}_7\text{Sb}_2\text{O}_{12}$). In order to identify various phases formed in the system, EDX analysis was carried out (Fig. 1). ZnO grains (Fig. 1a and b), bismuth rich phases at intergranular regions and at triple points (Fig. 1c and d) and antimony rich area (Fig. 1e and f) with a significant amount of zinc (possibly spinel phase $\text{Zn}_7\text{Sb}_2\text{O}_{12}$) were seen in the microstructure.

X-ray powder diffraction (XRD) measurements were carried out to identify the antimony and bismuth rich phases found by EDX analysis. X-ray diffraction results (Fig. 2) show that antimony rich area is $\text{Zn}_7\text{Sb}_2\text{O}_{12}$ and bismuth rich area is Bi_2O_3 (Refs. 2–5). Commercial samples also showed similar XRD patterns.

Electrical characterisation

Varistor discs obtained after a two stage sintering process ($1000^\circ\text{C}/0$ h; $900^\circ\text{C}/6$ h) were used for electrical studies. The current–voltage characteristics of nanosamples and commercial samples are given in Fig. 3. A steeper rise in voltage with current is obtained in varistors made from nanosize precursors compared with the commercial varistors. Most significantly, a considerably higher breakdown voltage is also found for the nanovaristor precursor samples sintered by these methods compared with the commercial sample made under the same experimental conditions. This is

Table 2 Breakdown voltages of varistor samples sintered at different temperatures

Sample	$V_c (\pm 30)$, V mm^{-1}
Commercial varistor ($1000^\circ\text{C}/0$ h; $900^\circ\text{C}/6$ h)	723
Nano varistor ($1000^\circ\text{C}/0$ h; $900^\circ\text{C}/6$ h)	1192
Commercial varistor ($1000^\circ\text{C}/2$ h)	584
Nanovaristor ($1000^\circ\text{C}/2$ h)	951

consistent with an increase in active grain boundaries present in the sintered nanomaterials.^{5–8}

These samples were also compared (Table 2) with those sintered at 1000°C and held for 2 h. Lower breakdown voltages were obtained for both commercial and nanosamples compared with the step sintered samples. Again, this behaviour may be attributed to the formation of more active grain boundaries.^{5–8}

Discussion

During sintering, various additives used in the varistor precursor get dispersed in such a way that grains become highly conductive and the grain boundaries highly resistive.^{1–7} High resistive grain boundaries therefore formed are responsible for obstructing conduction at low voltages and are the sources for non-linear electrical conduction at higher voltages. Grain size distribution plays a significant role in electrical behaviour and in particular, nanograin sized material exerts superior properties. In addition, it is well established that the breakdown voltage of a varistor is proportional to the number of grain boundaries.⁵ Based on the outlined information, the observed higher breakdown voltage of the varistors prepared from the nanosize powders (19 ± 3 nm) of the present study can be attributed to the increased number of grain boundaries formed as a result of smaller grain sizes arising from low temperature sintering. It is also plausible to assume that an increase in the number of grain boundaries leads to an increase in the number of active grain boundaries per unit volume, which again contributes to the higher breakdown voltage.^{12,13}

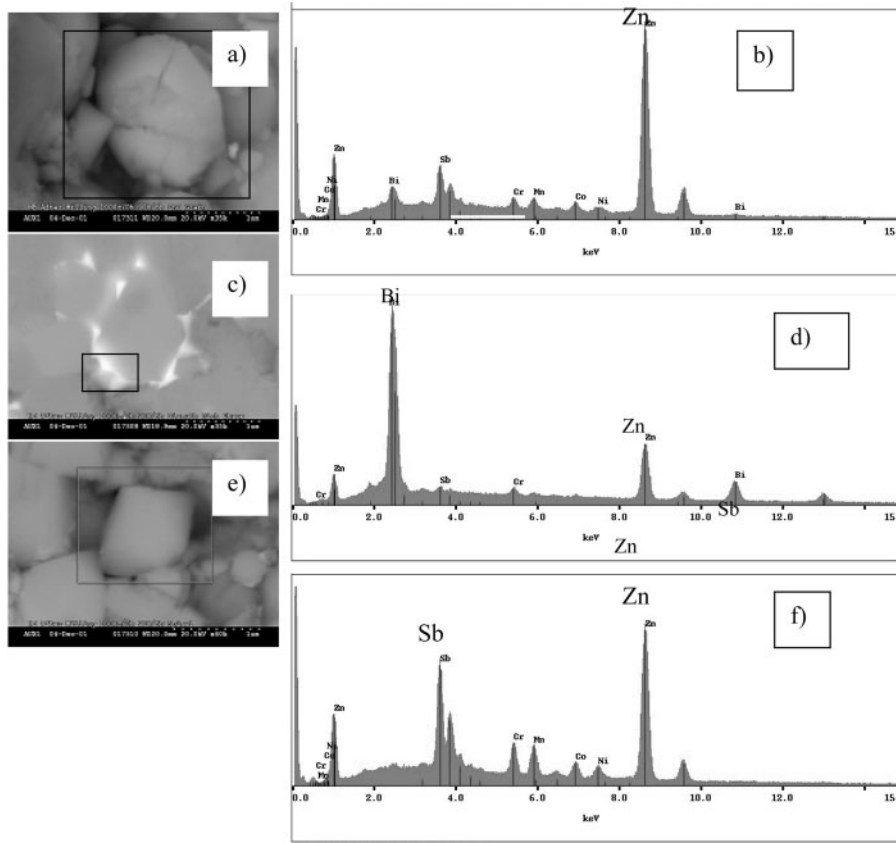
Conclusions

Controlling the varistor grain size at higher temperature is a real challenge in sintering varistor ceramics. In principle, the breakdown voltage could be increased very significantly if one could sinter the material so as to obtain submicrometre grain size.

The present study shows that working with nanosized precursors, it is possible to produce varistors with adequate density and enhanced electrical characteristics at temperatures substantially lower than those needed for conventional micrometre sized materials. Additionally, using the step sintering method, a varistor with higher performance characteristics is produced, illustrating the usefulness of this procedure. This however can again be

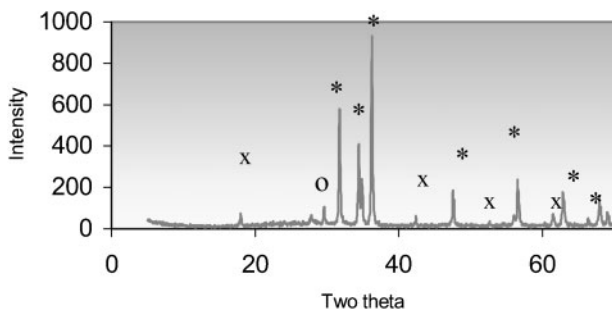
Table 1 Densification of varistor samples

Sample	Average density, g cm^{-3}	Density (± 0.3), %
Commercial varistor ($1000^\circ\text{C}/0$ h; $900^\circ\text{C}/6$ h)	5.17	92.2
Nano varistor ($1000^\circ\text{C}/0$ h; $900^\circ\text{C}/6$ h)	5.47	97.5
Commercial varistor ($1000^\circ\text{C}/2$ h)	5.30	94.7
Nanovaristor ($1000^\circ\text{C}/2$ h)	5.48	97.8

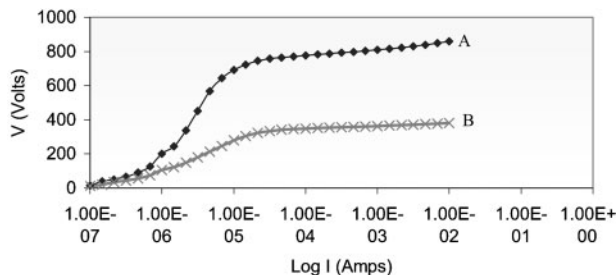


a and b ZnO grains; c and d bismuth rich (Bi_2O_3) area; e and f spinel phases

1 Field emission scanning electron microscopy and EDX



2 X-ray diffraction pattern of step sintered varistor samples prepared from nanosize precursors: *ZnO, x $\text{Zn}_7\text{Sb}_2\text{O}_{12}$ and o Bi_2O_3



3 I-V curve of varistor samples prepared by step sintering method (1000°C/0 h; 900°C/6 h): A – nanosamples, B – commercial samples (average thickness of pellets was 0.65 mm)

attributed to an increase in number of grain boundaries. Despite the success reported here, it is clear that an even greater improvement could be achieved if a sintering

method could be developed which would allow the maintenance of smaller particles. Other options are currently being explored to achieve this.

Acknowledgements

The authors gratefully acknowledge the financial support of HEA (PRTL Materials programme). The authors thank the Centre for Microscopy and Analysis, Trinity College Dublin and Mr. Kevin Travers, Littelfuse Ireland, for help with electrical measurements.

References

1. T. K. Gupta: *J. Am. Ceram. Soc.*, 1990, **73**, 1817–1840.
2. L. M. Levinson and H. R. Philip: *Ceram. Bull.*, 1986, **65**, 639–646.
3. M. Matsuoka: *Jpn J. Appl. Phys.*, 1971, **10**, 736–746.
4. G. H. Wiseman: *Key Eng. Mater.*, 1998, **150**, 209–218.
5. S. C. Pillai, J. M. Kelly, D. E. McCormack, P. O'Brien and R. Ramesh: *J. Mater. Chem.*, 2003, **13**, 2586–2590.
6. S. C. Pillai, J. M. Kelly, D. E. McCormack and R. Ramesh: *J. Mater. Chem.*, 2004, **14**, 1572–1578.
7. X. Ya, H. Yin, T. M. De and T. M. Jing: *Mater. Res. Bull.*, 1998, **33**, 1703–1708.
8. R. N. Viswanath, S. Ramasamy, R. Ramamoorthy, P. Jayavel and T. Nagarajan: *Nanostruct. Mater.*, 1995, **6**, 993–996.
9. I. W. Chen and X.-H. Wang: *Nature*, 2000, **404**, 168–171.
10. P. Duran, F. Capel, J. Tartaj and C. Moure: *J. Am. Ceram. Soc.*, 2001, **84**, 1661–1668.
11. P. Duran, F. Capel, J. Tartaj and C. Moure: *Adv. Mater.*, 2002, **14**, 137.
12. S. C. Pillai, J. M. Kelly, D. E. McCormack and R. Ramesh: *Mater. Sci. Technol.*, 2004, **20**, 964–968.
13. W. Z. Yang, D. L. Zhou, G. F. Yin, R. S. Wang and Y. Zhang: *J. Mater. Sci. Technol.*, 2005, **21**, 183–186.